


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)
Search: ☒ The ACM Digital Library ☐ The Guide



Searching within **The ACM Digital Library** for: non blocking transaction single synchroniz* ([start](#)
 Found **198** of **263,029**

REFINE YOUR SEARCH
[Search Results](#)
[Related Journals](#)
[Related Magazines](#)
[Related SI](#)

 Sort by [rel](#)
▼ Refine by Keywords

Discovered Terms
▼ Refine by People
[Names](#)
[Institutions](#)
[Authors](#)
[Reviewers](#)
▼ Refine by Publications
[Publication Year](#)
[Publication Names](#)
[ACM Publications](#)
[All Publications](#)
[Content Formats](#)
[Publishers](#)
▼ Refine by
[Conferences](#)
[Sponsors](#)
[Events](#)
[Proceeding Series](#)
ADVANCED SEARCH
[Advanced Search](#)
FEEDBACK

Please provide us with feedback

 Found **198** of **263,029**
Results 1 - 20 of 198
[Save results to a Binder](#)

 Result page: **1**
1 Transactional events

Kevin Donnelly, Matthew Fluet

 September 2006 **ICFP '06**: Proceedings of the eleventh ACM SIGPLAN inter programming

Publisher: ACM [Request Permissions](#)

Full text available: Pdf (264.80 KB)

 Additional Information: [full citation](#), [abst](#)
Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 43, Download

Concurrent programs require high-level abstractions in order to manage reasoning. In this paper, we introduce a novel concurrency abstraction, combines first-class synchronous messagepassing ...

Keywords: concurrency, first-class events, monads, synchronous mess

Also published in:

 September 2006 **SIGPLAN Notices** Volume 41 Issue 9

2 Deadlock detection in distribution object systems

Nima Kavah, Wolfgang Emmerich

 September 2001 **ESEC/FSE-9**: Proceedings of the 8th European software e ACM SIGSOFT international symposium on Foundations of

Publisher: ACM [Request Permissions](#)

Full text available: Pdf (198.67 KB)

 Additional Information: [full citation](#), [abst](#)
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 37, Downloa

The behaviour of a distributed system is largely determined by the use policies of the underlying middleware. The inherent parallel nature of di problems, such as deadlocks ...

Keywords: UML, model checking, object middleware, process algebra

Also published in:


 September 2001 **SIGSOFT Software Engineering Notes** Volume 26 Issue 5

3 Efficient fork-linearizable access to untrusted shared memory

Christian Cachin, Abhi Shetia, Alexander Shraer

 August 2007 **PODC '07**: Proceedings of the twenty-sixth annual ACM symp

Publisher: ACM  [Request Permissions](#)

Full text available:  Pdf (359.46 KB)

[Additional Information: full citation, abst](#)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 91, Downlo

When data is stored on a faulty server that is accessed concurrently by inconsistent data to different clients. For example, the server might cor respond with stale data ...


Keywords: arbitrary failures, fork-consistency, storage emulations

4 Checkpoint and Restart for Distributed Components in XCAT3

Sriram Krishnan, Dennis Gannon

November 2004 **GRID '04: Proceedings of the 5th IEEE/ACM International**

Publisher: IEEE Computer Society

Full text available:  Pdf (160.71 KB)


[Additional Information: full citation, abst](#)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 22, Downloa

With the advent of Grid computing, more and more high-end computati scientist. While this opens up new avenues for scientific research, it mal system a non-trivial ...


Keywords: Grids, Components, Web Services, Distributed Checkpointinr

5 Using elimination to implement scalable and lock-free FIFO queues

 Mark Moir, Daniel Nussbaum, Ori Shalev, Nir Shavit

July 2005 **SPAA '05: Proceedings of the seventeenth annual ACM symp architectures**

Publisher: ACM  [Request Permissions](#)

Full text available:  Pdf (196.23 KB)


[Additional Information: full citation, abst](#)

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 89, Downlo

This paper shows for the first time that elimination, a scaling technique structures, can be applied to FIFO data structures, specifically, to linear transform existing nonscalable ...


Keywords: FIFO queues, elimination, linearizability, lock-free, multipro scalability

6 Lazy argument passing in Java RMI

 Christopher Line, K. R. Jayaram, Patrick Eugster

September 2008 **PPPJ '08: Proceedings of the 6th international symposium in Java**

Publisher: ACM

Full text available:  Pdf (846.57 KB)

[Additional Information: full citation, abst](#)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 67, Downloa

Though often criticized for its inherent synchronization overhead and co

paradigm remains one of the most popular abstractions for building dist suggested ways to ...

Keywords: Java, argument passing, asynchronous, future, invocation,

7 Inferential queueing and speculative push for reducing critical comm



Ravi Rajwar, Alain Kägi, James R. Goodman

June 2003

ICS '03: Proceedings of the 17th annual international confere

Publisher: ACM



Request Permissions

Full text available: Pdf (568.93 KB)

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 28, Downloa

Communication latencies within critical sections constitute a major bottl workloads. In this paper, we argue for the use of Inferentially Queued L synchronization but also ...

Keywords: data forwarding, inferential queueing, synchronization

8 Architectural Support for Software Transactional Memory

Bratin Saha, Ali-Reza Adl-Tabatabai, Quinn Jacobson

December 2006 **MICRO 39**: Proceedings of the 39th Annual IEEE/ACM Inte

Publisher: IEEE Computer Society

Full text available: Pdf (325.24 KB)

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): 18, Downloads (12 Months): 180, Downl

Transactional memory provides a concurrency control mechanism that e synchronization. Researchers have proposed several different implemen classified into software transactional ...

9 Design tradeoffs in modern software transactional memory systems



Virendra J. Marathe, William N. Scherer, Michael L. Scott

October 2004 **LCR '04**: Proceedings of the 7th workshop on Workshop on le for scalable systems

Publisher: ACM

Full text available: Pdf (158.62 KB)

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 53, Downloa

Software Transactional Memory (STM) is a generic non-blocking synchr conversion of correct sequential objects into correct concurrent objects. traditional performance and ...

10 Software transactional memory for multicore embedded systems



Jennifer Mankin, David Kaeli, John Ardini

June 2009

LCTES '09: Proceedings of the 2009 ACM SIGPLAN/SIGBED c tools for embedded systems

Publisher: ACM



Request Permissions

Full text available: Pdf (443.92 KB)

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): 41, Downloads (12 Months): 167, Downl


Embedded systems, like general-purpose systems, can benefit from par platform. Unfortunately, concurrency issues present in general-purpose systems, protection from which is currently ...

Keywords: embedded systems, locking, multicore, software transaction transactions

Also published in:


June 2009 **SIGPLAN Notices** Volume 44 Issue 7

11 Constant-RMR implementations of CAS and other synchronization p

 Wojciech Golab, Vassos Hadzilacos, Danny Hendler, Philipp Woelfel

August 2007 **PODC '07: Proceedings of the twenty-sixth annual ACM symp**

Publisher: ACM  [Request Permissions](#)

Full text available:  Pdf (289.54 KB)

[Additional Information: full citation, abstr](#)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 31, Downloa

We consider asynchronous multiprocessors where processes communicate memory. We show how to implement consensus, all comparison primitives linked/store-conditional using only a constant ...


Keywords: comparison primitives, consensus, mutual exclusion, remot

12 Performance Evaluation of Task Pools Based on Hardware Synchron

Ralf Hoffmann, Matthias Korch, Thomas Rauber

November 2004 **SC '04: Proceedings of the 2004 ACM/IEEE conference on S**

Publisher: IEEE Computer Society


Full text available:  Pdf (208.41 KB)

[Additional Information: full citation, abstr](#)

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 35, Downlo


A task-based execution provides a universal approach to dynamic load t are arbitrary units of work that are created dynamically at run-time and the task pool, until ...

13 Robust implicit EDF: A wireless MAC protocol for collaborative real-t

 Tanya L. Crenshaw, Spencer Hoke, Ajay Tirumala, Marco Ceccame

September 2007 **Transactions on Embedded Computing Systems (TEC**

Publisher: ACM  [Request Permissions](#)

Full text available:  Pdf (663.47 KB)

[Additional Information: full citation, abstr](#)

Bibliometrics: Downloads (6 Weeks): 19, Downloads (12 Months): 111, Downl

Advances in wireless technology have brought us closer to extensive de systems connected through a wireless channel. The medium-access control providing a real-time guarantee. ...

Keywords: Earliest deadline first, medium-access control, real time, wi

**Deriving linearizable fine-grained concurrent objects**

Martin Vechev, Eran Yahav

June 2008 **PLDI '08**: Proceedings of the 2008 ACM SIGPLAN conference implementation**Publisher:** ACM[Request Permissions](#)Full text available: [Pdf](#) (935.82 KB)Additional Information: [full citation](#), [abstract](#)**Bibliometrics:** Downloads (6 Weeks): 13, Downloads (12 Months): 140, Downloads (Since Publication): 140

Practical and efficient algorithms for concurrent data structures are difficult to design. The literature are often optimized for a specific setting, making it hard to implement a general-purpose ...

Keywords: algorithms, concurrency, data structures, linearizability, memory management

Also published in:

May 2008 **SIGPLAN Notices** Volume 43 Issue 6**15 Aggressive snoop reduction for synchronized producer-consumer code****embedded multi-processors**

Chenjie Yu, Peter Petkov

September 2007 **CODES+ ISSS '07**: Proceedings of the 5th IEEE/ACM international conference on code design and system synthesis**Publisher:** ACMFull text available: [Pdf](#) (163.62 KB)Additional Information: [full citation](#), [abstract](#)**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 41, Downloads (Since Publication): 41

Snoop-based cache coherence protocols are typically used when multiple processors share a common bus. It is well known, however, that these coherence protocols help alleviate this problem, ...

Keywords: cache coherence, embedded systems, low-power multiprocessors**16 Nonblocking k-compare-single-swap**




Victor Luchangco, Mark Moir, Nir Shavit

June 2003 **SPAA '03**: Proceedings of the fifteenth annual ACM symposium on parallel algorithms and architectures**Publisher:** ACM[Request Permissions](#)Full text available: [Pdf](#) (197.17 KB)Additional Information: [full citation](#), [abstract](#)**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 41, Downloads (Since Publication): 41

The current literature offers two extremes of nonblocking software synchronization: intricate designs of specific structures based on single-compare-and-swap (CAS), and general-purpose ...





Keywords: concurrent data structures, linked lists, multiprocessors, non-blocking algorithms**17 Practice of parallelizing network applications on multi-core architectures**

Junchang Wang, Haipeng Cheng, Bei Hua, Xinan Tang

- June 2009 **ICS '09**: Proceedings of the 23rd international conference on
 **Publisher:** ACM  [Request Permissions](#)
 Full text available:  [Pdf](#) (1.05 MB) **Additional Information:** [full citation](#), [abstract](#)
Bibliometrics: Downloads (6 Weeks): 58, Downloads (12 Months): 154, Download

The industry wide shift to multi-core architectures arouses great interest. However, it is very difficult to parallelize fine-grained applications for multi-processor hardware support ...

Keywords: application-level protocol processing, deep content inspection, hardware parallelization, pipelining implementation, tcp/ip protocol processing



- 18 **Parallelizing security checks on commodity hardware**
 Edmund B. Nightingale, Daniel Peek, Peter M. Chen, Jason Flinn
 March 2008 **ASPLOS XIII**: Proceedings of the 13th international conference on computer programming languages and operating systems
Publisher: ACM  [Request Permissions](#)
 Full text available:  [FLV](#) (26:0 MIN),  [Pdf](#) (306.87 KB) **Additional Information:** [full citation](#), [abstract](#)
Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 194, Download

Speck (Speculative Parallel Check) is a system that accelerates powerful security checks by executing them in parallel on multiple cores. Speck provides an infrastructure for analyzing particular ...

Keywords: operating systems, parallel, performance, security, speculation

Also published in:

- | | | |
|------------|---|-------------------|
| March 2008 | SIGPLAN Notices | Volume 43 Issue 3 |
| March 2008 | SIGARCH Computer Architecture News | Volume 36 Issue 1 |
| March 2008 | SIGOPS Operating Systems Review | Volume 42 Issue 2 |

- 19 **Data sharing protocols for SMT processors**
 Shi-Wu Lo
 April 2006 **SAC '06**: Proceedings of the 2006 ACM symposium on Applied computing
Publisher: ACM  [Request Permissions](#)
 Full text available:  [Pdf](#) (197.60 KB) **Additional Information:** [full citation](#), [abstract](#)
Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 18, Download

Although there are many real-time task synchronization protocols designed for multiprocessor systems, most of them do not fit the needs in accommodating *simultaneous* task synchronization protocols are ...

Keywords: real-time, scheduling, simultaneously multithreading

- 20 **Improving instruction cache performance in OLTP**
 Stavros Harizopoulos, Anastassia Ailamaki
 September 2006 **Transactions on Database Systems (TODS)**, Volume 31

Publisher: ACM  [Request Permissions](#)

Full text available:  [Pdf](#) (783.16 KB)

[Additional Information: full citation, abstr](#)

Bibliometrics: Downloads (6 Weeks): 13, Downloads (12 Months): 105, Downl

Instruction-cache misses account for up to 40&percent; of execution time database workloads. In contrast to data cache misses, instruction misse execution. Chip design limitations ...

Keywords: Instruction cache, cache misses

Result page: 1

The ACM Portal is published by the Association for Computing Machinery. Copyright ©

[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  [Adobe Acrobat](#)  [QuickTime](#)  [Windows Media Player](#)